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Process Optimization to Eliminate Automatic Alignment Failures on the Scalable Device

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

The paper focused in addressing the auto align defect at in-strip testing of a semiconductor scalable device in a leadframe technology. Pareto diagram and potential risk analysis were completed to identify the top reject contributors and eventually come-up with the robust solution. Reverse flow was employed to eliminate the alignment issues. The reverse flow, which is testing prior singulation process, eventually resolved the auto align and other singulation related defects as testing is done on a strip form. Ultimately, the error-proofing or Poka-Yoke approach by reverse flow lead to the elimination of auto align failures at final test. For future works, the parameters and learnings could be used on devices with similar assembly defect occurrence.

Keywords: Auto align; leadframe; semiconductor; test process; singulation.

1. INTRODUCTION

Continuous development and new trends in semiconductor technology come along few to many challenges in assembly manufacturing. An important mission for a semiconductor industry is to sustain its competitive market value and position. Important to note that failure to deliver customer requirements and expectation would result to non-design win, missed opportunities, and possible business failure. This situation should be necessarily avoided that is why after product qualification, line-stressing is being employed in preparation to mass-production mode [1,2].

Around 10-30 lots are line-stressed to capture all hindrances in the production line and thus corrected immediately to prevent quality and delivery issues of the device. The device in focus is a scalable device utilizing a leadframe technology. Top rejects were identified on critical processes that substantially affecting the delivery and yield during line-stressing. With this, process optimization is highly recommended before it reaches the mass-production release.

2. EXPERIMENTATION

A complete process flow for the device in focus is given in Fig. 1. Worthy to mention that the

process flow varies depending on the product and the technology [1-5]. With the continuing technology development and state-of-the-art platforms, challenges in semiconductor industry are inexorable [6-9].

Assembly process defects were encountered during the line-stressing and ramp-up of the device. Critical processes were determined using risk analysis, and one of which focused on the instrip testing process (simply test process) as shown in Table 1. Evaluation was done before the risk build to promote confidence on line-stressing. Moreover, potential risk analysis was given contingency plans and established corrective actions.

Reject contributors per critical process are shown in Fig. 2. Test process is one critical process identified with output abnormalities as a result of unoptimized parameters which are normally attributed to newly-introduced devices. Moreover, test process contributed to the 36% defects, which is the highest percentage as highlighted the defect contribution chart.

For the test process defect contribution, pareto diagram in Fig. 3 shows auto align failures as the top reject parts per million (ppm) contributor. Parameter optimization is one of the factors to be checked as the device in focus has no

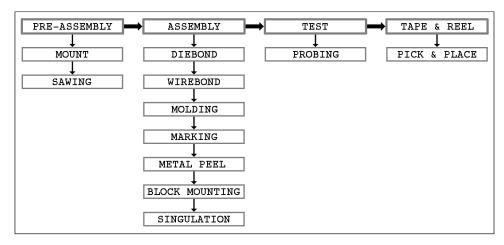


Fig. 1. Assembly manufacturing process flow

Table 1. Potential risk analysis at test process

Identified risk	Resulting	Resulting Evaluation before action			Identified action	
	potential risk	Probability	Impact	Class	•	
In-strip test over-rejections (singulated units)	Low yieldReliability	9	9	Α	Implementation of reverse process flow	

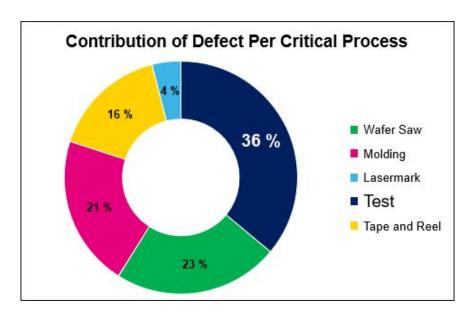


Fig. 2. Defect contribution per assembly process

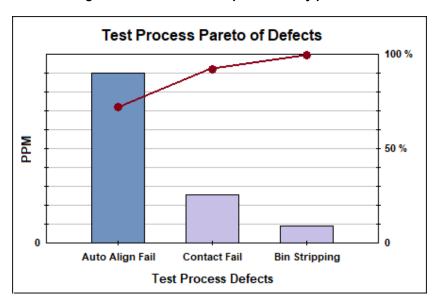


Fig. 3. Pareto diagram of rejects showing the top contributor

other similar product in the plant as reference. Benchmarking on other sites is being considered to have a baseline for critical process parameters.

Top rejects based on pareto diagram greatly affect the delivery and yield during production stressing performance. Henceforth, process optimization is critically needed at line-stressing before the mass-production release. Table 2 shows the top defect signature of the test process. Succeeding analysis and investigation of failures were employed by collecting the actual

reject samples, which are crucial in formulation of corrective actions and improvement.

Units are normally tested after singulation but in limited quantity. Singulation is the process of cutting into individual or singular units from a leadframe strip. In this era of technological advancement of high-density device, in-strip testing was developed. The problem however is the contacting issues in Fig. 4. The device is comprised of 12,740 singulated units making it prone to alignment failures compared to other devices consisting of less than 500 units.

Table 2. Top defect signature at test process

Critical process	Top defect signature	Criteria	Remarks
Test process	Auto align failure	Not allowed	Failed

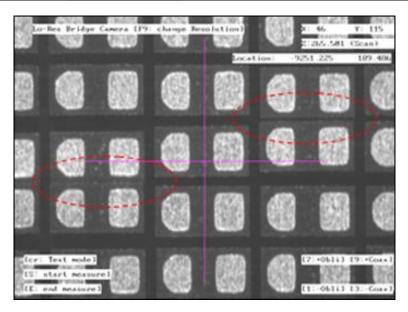


Fig. 4. Singulated units showing some narrow gaps, resulting to auto align failures

3. METHODOLOGY

To mitigate or eliminate alignment issues, reverse flow was employed. The reverse flow which is testing prior singulation process will ultimately resolve the auto align failures and other singulation related defects as testing will be done on a strip form. Table 3 gives the matrix to help identify and address the auto align failure.

4. RESULTS AND DISCUSSION

Optimized process parameters were attained based on the results of the evaluation that addressed the top reject contributor of the test process. Comparative tests and analysis were used to statistically validate the results. Fig. 5 shows the comparable yield and test results during preliminary evaluations when reverse flow is implemented without auto align failures.

Though preliminary evaluations were made, large scale validation is still needed as reverse

flow is considered major change and will undergo process change review. It will take a longer time to implement due to its major change requirements. Auto align failures were still further investigated while waiting for the reverse flow to be put in place. Cause and effect matrix was tabulated to identify other factors contributing to this defect.

Solution and error proofing shared in Table 4 were formulated after identifying the potential causes and validating its contribution on auto align failures. Solution was put in place based on cost, applicability, effectiveness and impact to the problem. During the course of brainstorming, a breakthrough idea came out that will defeat all odds. Auto align failures would ultimately resolve by reversing its process, as auto align failures occur when the products are singulated brought about by conventional way of testing units after singulation process, this time testing was done on a strip form prior singulation thus eliminating the problem.

After the implementation of the identified solutions, level of rejections was monitored. Shown below in Fig. 6 are the results before and after the solution implementation, with actual values intentionally not given. Regardless, percentage comparison is provided.

An error-proofing or Poka-Yoke approach by reverse flow lead to the elimination of auto align failures and hence a remarkable improvement of 100% gained after the implementation of corrective actions. This is an acceptable indication of manufacturing preparedness for mass-production mode.

Table 3. Matrix to address auto align failures, with significant factors denoted in*

Man	Machine	Method	Material	Environment
Prober operator	Prober	Strip loading *	Strip *	N/A
Singulation operator	Sawing machine	Strip sawing *	Blade	N/A
Strip mount operator	Strip mounter	Strip mounting *	Mounting tape Mounting jig *	N/A
·		Sawing before testing *		N/A

		Wafer	Gross	Pass	Yield	Fail	Bin 1	Bin 5	Bin 7	Bin 14
singulated un-singulated	1	12736	12720	99.87%	16	12720	0	0	16	
	2	12736	12709	99.79%	27	12709	5	0	22	
	3	12736	12725	99.91%	11	12725	1	0	10	
	4	12736	12710	99.80%	26	12710	0	ୀ	25	
	. 1	12736	12716	99.84%	20	12716	0	0	20	
	2	12736	12703	99.74%	33	12703	6	0	27	
	3	12736	12717	99.85%	19	12717	1	0	18	
	4	12736	12570	98.70%	166	12570	4	1	161	

Fig. 5. Yield comparison of un-singulated vs. singulated units causing auto align fails

Table 4. Solution validation matrix

Potential causes	Actions	Error proofing level	Status
Excessive vacuum force on prober chuck	Install air regulator / vacuum reducer near chuck area	2	Implemented
Insufficient edge stopper to prevent block from moving during mounting	Redesign mounting jig with edge stopper to prevent block from moving during mounting	2	Implemented
Too many air voids in between unit and tape upon mounting	Cleaning of block prior mounting	3	Implemented
Movement of singulated units causing AA failures	Implementation of reverse flow Implement testing prior singulation process	1	Implemented

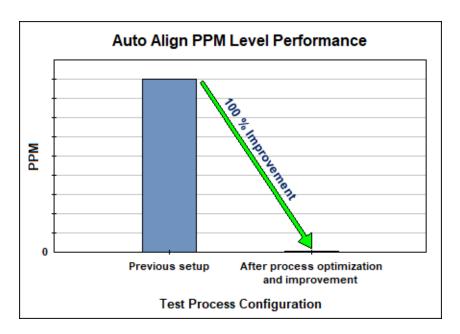


Fig. 6. Improvement after optimization and implementation of corrective actions

5. CONCLUSIONS AND RECOMMENDA-TIONS

Thorough evaluations with the aid of statistical analysis were done in solving and addressing the test auto align failures of a scalable device. Test process optimization was formulated with the reverse flow method performed, resulting to successful elimination of the auto align failures.

Process optimization plays a crucial role to as early as product qualification and line-stressing stage before mass-production release can be approved. Techniques and learnings shared in this paper could be used on other works with similar requirement. Moreover, works and studies discussed in [10,11] are helpful in improving the assembly processes particularly in the yield improvement.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

- May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st Ed., Wiley-IEEE Press, USA; 2006.
- Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
- 3. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
- Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA; 2016.

- Harper C. Electronic packaging and interconnection handbook. 4th Ed., McGraw-Hill Education, USA; 2004.
- Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008;1-11.
- Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference. Malaysia. 2012;1-5.
- Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
- Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging. Taiwan. 2002;1-6.
- Gomez FR, Mangaoang Jr. T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-MR leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.
- Sumagpang Jr. A, Gomez FR, Rodriguez R. Tool setup improvement for package scratch mitigation at end-of-line process. Journal of Engineering Research and Reports. 2020;12(3):1-5.

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