Physical Review & Research International
3(4): 568-576, 2013

SCIENCEDOMAIN *international*
www.sciencedomain.org

Simulation Study of Circuit Performance of GAA Silicon Nanowire Transistor and DG MOSFET

Reza Hosseini[1*] and Neda Teimuorzadeh[1]

[1]Department of Electrical Engineering, Khoy Branch, Islamic Azad University, Khoy, Iran.

Authors' contributions

This work was carried out in collaboration between all authors. All authors read and approved the final manuscript.

Research Article

Received 12th March 2013
Accepted 17th July 2013
Published 24th July 2013

ABSTRACT

In this paper, electrical characteristics of Double Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET) and that of Gate All Around Silicon Nanowire Transistor (GAA SNWT) were investigated. In particular, the effect of channel length was studied. Full quantum mechanical models theoretically are the most accurate way to study such ultrasmall nanodevices. Phenomenological quantum correction model, a calibrated 3D density gradient model, was adopted in this work. Furthermore, we presented the operations of associated CMOS inverter, which were investigated in terms of static power dissipation and propagation delay. We also compared the operation of GAA SNWT inverter with that of DG MOSFET. Simulated static power dissipation and propagation delay of the GAA SNWT inverter were found to be about 17nW and 14ps, respectively, compared with 10μW and 16ps achievable with DG MOSFET inverter.

Keywords: DG MOSFET; GAA SNWT; density gradient model; CMOS inverter.

1. INTRODUCTION

Scaling the transistor sizes has made significant improvement in the cost effectiveness and performance of integrated circuit over the last few decades. The bulk CMOS technology is rapidly approaching the scaling limit and hence alternate device structures are essential for

[*]Corresponding author: Email: hosseini@iaukhoy.ac.ir;

future electronic devices. Thus, various device concepts such as double-gate MOSFETs (DG MOSFETs) and gate all around silicon nanowire transistors (GAA SNWTs) are becoming extensively attractive [1-4].

The major problem of the continuous scaling is the so-called short-channel effects (SCEs) affecting the current drivability of the devices. The great advantage of the multi-gate devices over single-gate devices is the excellent control of SCEs in sub-15 nm gate lengths.In addition, these devices exhibit a good I_{on}/I_{off} and present a channel with high conductivity [5-6]. GAA SNWTs have emerged as promising devices for nano-scale circuits due to their better scalability below 15 nm in compared to DG MOSFETs. Due to the presence of gate all around, the effective gate control increases, reducing DIBL [7]. Also, the use of a lightly doped or undoped channel is desirable for immunity against dopant fluctuation effects which give rise to threshold-voltage variation, and also for reduced drain-to body capacitance and higher carrier mobility which provide improved circuit performance [8].

In this paper, we have explored the possibility of designing a nanoscale inverter with a reduced delay time and power consumption. In the study, a CMOS inverter designed with a GAA SNWT has been compared with a DG MOSFET of similar dimension. Phenomenological quantum correction model, a calibrated 3D density gradient model, has been adopted in this work. This paper is organized as follows: section 2 describes structure of presented devices. Section 3 presents the simulation method. Section 4 compares the electrical characteristics of GAA SNWT with that of DG MOSFET. Section 5 summarizes key findings of this work.

2. DEVICE STRUCTURE

2.1 DG MOSFET

The DGMOSFET structure studied here is presented in Fig. 1. The channel of device is intrinsic silicon, source and drain are highly doped(N_D= 10^{20} cm^{-3}) and those are in the same length ($L_{S,D}$=6.5nm). Device employs a midgap metal gate (Φ_M = 4.7eV) with lateral SiO_2 spacers partially covering source and drain regions. In this study, body length (T_{Si}) is assumed 5nm and channel length (L_{ch}) varies from 7nm to 25nm and the oxide thickness (T_{ox}) is 1.5nm.

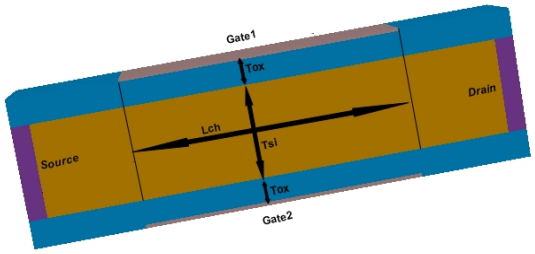
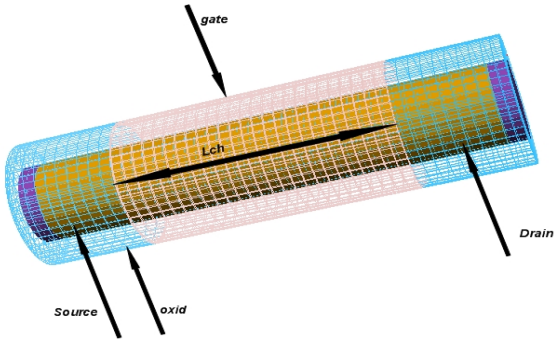


Fig. 1. DG MOSFET simulated in this paper

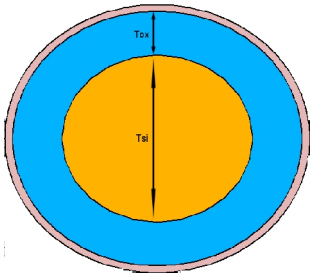
2.2 GAA SNWT

The GAA SNWT structure studied in this work is shown in Fig. 2. The channel length varies from 7nm to 25 nm. SNWT's radius is 2.5nm and oxide thickness (T_{ox}) is 1.5nm. Similar to

DG MOSFET, the channel of GAA SNWT is intrinsic silicon, source and drain are highly doped(N_D= 10^{20} cm^{-3}) and those are in the same length($L_{S,D}$=6.5nm).The workfunction of metal gate is 4.7eV. For this device, we provide electrical characteristics and compare them with those of DG MOSFET.



(a)



(b)

Fig. 2. GAA SNWT simulated in this paper. a) schematic view b) Cross-section of simulated GAA SNWT

3. SIMULATION METHOD

In the nanometer regime, the wave-like behavior of electron becomes significant, and the tunneling current should be considered. The effects due to confinement of carriers associated with variations of local potential on the scale of the electron wave functions (i.e.,quantum effects) can be modeled using density gradient [9].

For the solution of the density gradient corrected drift diffusion approximation, we use a modified Gummel approach [10] where the Poisson equation (1) and Density Gradient equation (2), for a given electron Fermi-level distribution, are solved self-consistently for the electrostatic potential and the quantum-corrected electron density [11]:

$$\nabla.(\varepsilon\nabla\psi) = -q(p - n + N_D^+ - N_A^-) \quad (1)$$

$$\frac{2b_n^*}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2}+\frac{1}{m_y}\frac{\partial^2 S}{\partial y^2}+\frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right)=\phi_n-\psi+\frac{K_B T}{q}\ln\left(S^2\right) \tag{2}$$

where $S=\sqrt{n/n_i}$, $b_n^*=\hbar/4qr$, Φ_n is quasi Fermi level, ψ is the electrostatic potential, ε is the local permittivity, K_B is Boltzmanns constant, T is lattice temperature and m is carrier effective mass. Equation (2) is the anisotropic density gradient equation [12], so there are different effective mass components in the transport (longitudinal) direction from in the confinement (transverse) direction.

The effective quantum-corrected potential is then calculated from [11]:

$$\psi_{eff}=\psi+\frac{2b_n^*}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2}+\frac{1}{m_y}\frac{\partial^2 S}{\partial y^2}+\frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right)=\phi_n+\frac{K_B T}{q}\ln\left(S^2\right) \tag{3}$$

and is then used as the driving potential for the current continuity equation:

$$\nabla . J_n=0 \tag{4}$$

where

$$J_n=-qn\mu_n\nabla\psi_{eff}+qD_n\nabla n \tag{5}$$

Which is solved using a standard Sharfetter-Gummel discretisation based on the effective quatum-corrected potential. The set of equations are solved using ATLAS simulator [13-14]. The standard concentration dependent mobility, parallel field mobility, Shockley-Read-Hall recombination with fixed carrier lifetimes, Fermi Dirac statistics models are used in our analysis. The system of equations (1,2 and 4) are solved self consistently until convergence. Dirichlet boundary condition is used for the source and drain contacts.

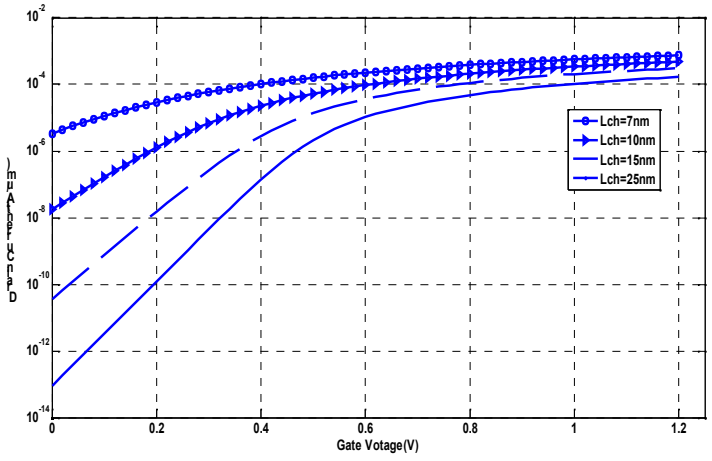


Fig. 3. Drain current versus gate voltage for DGMOSFET when channel length varies from 7nm to 25 nm and V_{DS}=0.5V

4. RESULTS AND DISSCUSSION

Fig. 3 represents the source - drain current as a function of gate voltage for DG MOSFET when V_{DS} = 0.5V and channel length varies from 7nm to 25 nm. Similar I-V characteristic for GAA SNWT are shown in Fig. 4. It can be seen that the reduction of the channel length results in shifting the characteristics to the left and it is clear that as the channel length becomes smaller than 15nm, the subthreshold current rises dramatically. Since the drain current depends on the channel length, the threshold voltage of the DG MOSFET and GAA SNWT should also be channel length dependent.

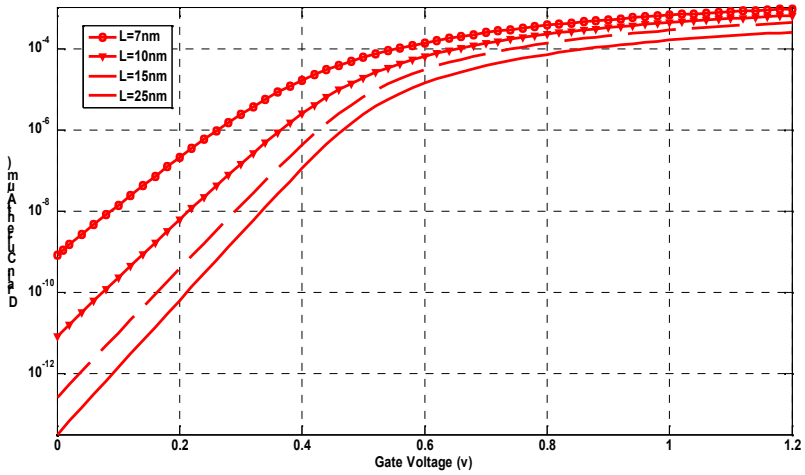


Fig. 4. Drain current versus gate voltage for GAA SNW Transistor when channel length varies from 7nm to 25 nm and V_{DS}=0.5V

Electrical characteristics of DG MOSFET and GAA SNWT are summarized in Table 1 and Table 2. The threshold voltage is calculated from the device I-V characteristics. We define the threshold voltage as the gate voltage at which the drain current becomes 0.1μA at V_{DS}=0.5V. It shows that threshold voltage decreases with reduction of channel length.

Table 1. Simulation results for DG MOSFET

	L_{ch}=7nm	L_{ch}=10nm	L_{ch}=15nm	L_{ch}=25nm
Threshold Voltage(V)	0.153	0.261	0.342	0.401
Subthreshol Slope(mV/dec)	150	127	105	66
DIBL	0.368	0.262	0.177	0.130
ON Current (A/μm)	2.45×10^{-4}	1.83×10^{-4}	1.28×10^{-4}	9×10^{-5}
OFF Current (A/μm)	9×10^{-7}	6.9×10^{-8}	2.58×10^{-8}	5×10^{-10}

Table 2. Simulation results for GAA SNWT

	L_{ch}=7nm	L_{ch}=10nm	L_{ch}=15nm	L_{ch}=25nm
Threshold Voltage(V)	0.304	0.350	0.384	0.409
Subthreshol Slope(mV/dec)	97	86	70	65
DIBL	0.238	0.198	0.159	0.130
ON Current (A/μm)	3.91×10^{-4}	2.9×10^{-4}	1.99×10^{-4}	1.2×10^{-4}
OFF Current (A/μm)	1.44×10^{-8}	1×10^{-9}	1.88×10^{-10}	6.4×10^{-11}

In Table.1, ON and OFF currents are given for DG MOSFET and in Table. 2 those are given for GAA SNWT. ON current is computed current at V_{DS}=0.5V and V_{GS}-V_{TH}=0.5V. OFF current is computed current at V_{DS}=0.5V and V_{GS}-V_{TH}=-0.2V [15-16]. It is observed I_{ON} does not vary significantly with channel length but I_{OFF} changes sharply. I_{OFF} is affected by quantum tunneling for L< 15nm and is heavily dependent on the channel length. Such dependence is mainly due to the degradation of the subthreshold slope with decreasing channel length. Furthermore, the OFF current in GAA SNWT is less than that in DG MOSFET because of smaller Subthreshold Slope.

Table.1 and Table. 2 also show the effect of varying the channel length on the DIBL. Above 15nm, the DIBL is relatively the same, but DG MOSFET with L_{ch} less than 15nm presents significant DIBL effect in comparison with GAA SNWT. This is attributed to the higher gate control in GAA SNWT. Another important parameter characterizing the short channel performance is the Subthreshold Slope (SS). A decrease in the channel length causes Subthreshold Slope to increase. On the other hand, increasing the gate control, reduces the subthreshold slope. It provides ideal sub-threshold slope and DIBL in the short devices.

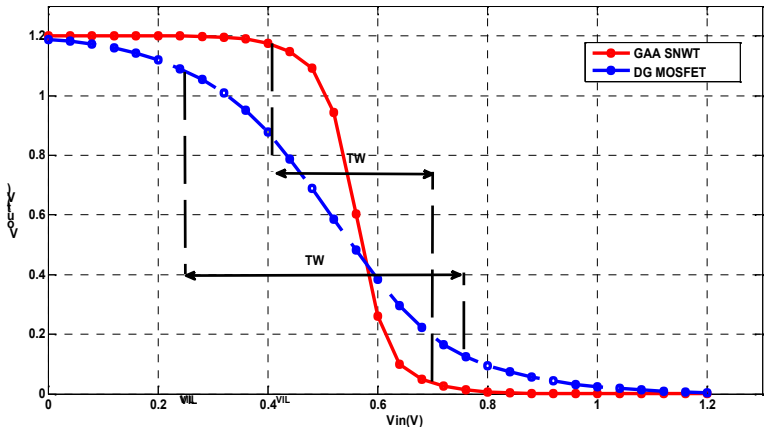


Fig. 5. Voltage Transfer Characteristic of DG MOSFET and GAA SNWT inverters comparing transition rates when Lch=7nm

Fig. 5 shows the Voltage Transfer Characteristics (VTC) of CMOS inverter designed with both the GAA SNWT and DG MOSFET. The structure and characteristics of PMOS in inverters are the same as NMOS with source/drain doping N_A= 10^{20} cm^{-3}. Also the load capacitance value is 5fF. We can see the advantages of the GAA SNWT inverter by comparing the transition width and noise margin of the circuitry of both [17]. The transition

width ($TW=V_{IH}-V_{IL}$) of the inverter with the GAA SNWT is 0.3V,whereas that of the inverter with the DG MOSFET is 0.5V. For GAA SNWT inverter, noise margin high ($NMH=V_{OH}-V_{IH}$) reaches 0.507 V, and noise margin low ($NML=V_{IL}-V_{OL}$) reaches 0.411 V. From Fig.5, we can also see NMH=0.425 V and NML=0.248 V for DG MOSFET inverter. Low transition width and high noise margin have been observed in GAA SNWT inverter.

Fig. 6 compares the transient responses of the inverters in terms of the propagation delay. The rise and fall times of input pulse is 1ps with 20ps pulse width. The propagation delay of the CMOS inverter using GAA SNWT is 14ps and it is 16ps for the other. The static power dissipation for CMOS inverter using DG MOSFET and GAA SNWT are also investigated. The inverter made by GAA SNWT has the static power dissipation less than the other in the short channel regime. It is 17nW for GAA SNWT inverter and 10μW for DG MOSFET inverter. It is apparent that for the length smaller than 15nm, GAA SNWT is an excellent candidate for digital application.

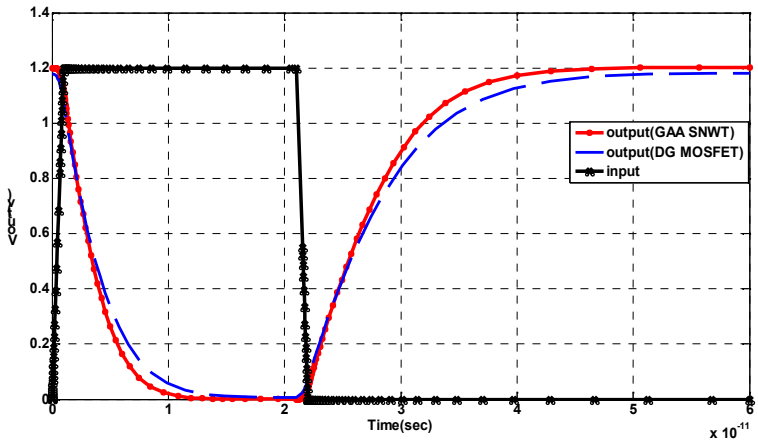


Fig. 6. Transient response of the inverters with DGMOSFET and GAA SNWT

5. CONCLUSION

In this paper, we have analyzed the electrical characteristics of DG MOSFET and GAA SNW transistor. A quantum correction model based on density gradient model was implemented in these devices. When channel length decreases, short channel effects will be more important but we can decrease these effects by using the device which has a good control of gate. We showed that the GAA SNWT had very good control of gate leading to lower DIBL effect, lower sub-threshold slope and higher ON current and lower OFF current.

We used these devices in CMOS inverter. Low transition width and high noise margin were observed in GAA SNWT inverter. GAA SNWT degraded static power dissipation and improved propagation delay. The analysis presented here decisively confirms that the application of the GAA SNTW in the switching circuits will meet the requirements in designing nanoscale devices with low static power dissipation and enhanced speed.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Loussier X, Munteanu D, Autran J, Simulation study of circuit performances of independent double-gate (IDG) MOSFETs with high- permittivity gate dielectrics. Journal of Non-Crystalline Solids. 2009;355:1185-1188
2. Jandhyala S, Kashyap R, Anghel C, Mahapatra S. A Simple Charge Model for Symmetric Double-Gate MOSFETs Adapted to Gate-Oxide-Thickness Asymmetry, IEEE Transaction of Electron Device. 2012;59(4):1002-1007
3. Seonghoon J, Chan Hyeong P, In-Young Ch, Young J,and Hong S, NANOCAD Framework for Simulation of Quantum Effects in Nanoscale MOSFET Devices, Journal of Semiconductor Technology and Science. 2006;6(1):1-9
4. Shin M, Efficient Simulation of Silicon Nanowire Field Effect Transistors and their Scaling Behavior, Journal of Applied Physics. 2007;101:024510
5. Kolberg S, Borli H, Fjeldly T, Modeling, Verification and Comparison of Short channel Double Gate and Gate-all-around MOSFETs', Mathematics and Computers in Simulation. 2008; 79:1107–1115.
6. Nirmal D, Vijayakumar P, Shruti K, Mohankumar N, Nanoscale channel engineered double gate MOSFET for mixed signal applications using high-k dielectric, International Journal of Circuit Theory and Applications; 2012, DOI: 10.1002/cta.1800
7. Hosseini R, Fathipour M, Faez R. Quantum simulation study of gate-all-around (GAA) silicon nanowire transistor and double gate metal oxide semiconductor field effect transistor (DG MOSFET). International Journal of the Physical Sciences. 2012;7(28):5054-5061.
8. Xiao D, Wang X, Yu Y, Chen J, Zhang M, Xue Z, Luo J, TCAD Study on Gate-All-Around Cylindrical (GAAC) Transistor for CMOS Scaling to the End of the Roadmap. Microelectronic Journal. 2009;40:1766–1771.
9. Ferron A, Cottle B, Curatola G, Fiori G, Guichard E, Schrödinger Approach and Density Gradient Model for Quantum Effects Modeling, A Journal for Process and Device Engineers. 2004;14:1-3
10. Wettstein A, Schenk, Fichtner W. Quantum Device-Simulation with the Density Gradient Model on Unstructured Grids, IEEE Transaction on Electron Devices. 2001;48:279-283.
11. Brown A, Martinez A, Seoane N, Asenow A. Comparison of Density Gradient and NEGF for 3D Simulation of a Nanowire MOSFET, Proceeding of the 2009 Spanish Conference on Electron Devices. 2009;140-143.
12. Sampedro C, Gamiz F, Godoy A, Garcia F, The Multi valley Effective Conduction Band-Edge Method for Monte Carlo Simulation of Nanoscale Structures, IEEE Transaction on Electron Device. 2006;53:2703-2710
13. Kumar P, Jit S. A Subthreshold Swing Model for Symmetric Double-Gate (DG) MOSFETs with Vertical Gaussian Doping, Journal of Semiconductor Technology and Science. 2010;10(2):107-117
14. Atlas User Manual, Device Simulation Software; 2011.
15. Young J, Young W, Park J, Lee J , Park B, Design Optimization of Gate-All-Around (GAA) MOSFETs, IEEE Transactions on Nanotechnology. 2006;5:186-191

16. Alam K, Abdullah M, Effects of dielectric constant on the performance of a gate all around InAs nanowire transistor, IEEE Transaction on Nanotechnology. 2012;11:82-87.
17. Seyedi A, Pavel A, Sharma A, Islam N, Design and performance analysis of a nanoscaled inverter based on wraped-around-gate nanowire MOSFETs, Micro & Nano letters. 2009;4:16-21

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sciencedomain.org/review-history.php?iid=224&id=4&aid=1731